CLAIMS

What is claimed is:

1. A process of forming a refractory metal liner, comprising:

depositing a layer of refractory metal on a first conductive layer, at least half of said depositing being carried out in the presence of an amount of passivating agent that is sufficient to impede subsequent reaction of at least a top half of said layer of refractory metal with said first conductive layer and is less than an amount of passivating agent necessary to form a stoichiometric refractory metal compound with said passivating agent; and

annealing said refractory metal and said first conductive layer in a first element ambient, thereby forming a stoichiometric refractory metal with said first element in at least a portion of said top half of said layer of refractory metal.

2. The process in claim 1, wherein said depositing step forms a barrier in a central portion of said layer of refractory metal.

3. The process in claim 2, wherein said barrier impedes impurities from diffusing through said layer of refractory metal during said annealing process.

4. The process in claim 3, wherein said impurities comprise silicon impurities.

5. The process in claim 2, further comprising forming a second conductive layer over said layer of refractory metal in a chemical vapor deposition process, wherein said barrier impedes impurities from diffusing through said layer of refractory metal during said chemical vapor deposition process.

6. The process in claim 5, wherein said impurities comprise fluorine impurities.

7. The process in claim 1, wherein:

said refractory metal comprises one of tungsten, titanum, molybdenum and nickel;

said passivating agent comprises one or more of nitrogen and chlorine; and

said first element comprises one or more of hydrogen, nitrogen, and ammonia.

8. A process of forming an electrical connection in an integrated circuit chip, said process comprising:

depositing a liner on a first conductive layer, a portion of said depositing being carried out in the presence of a passivating material, wherein said

passivating material combines with said liner to form a barrier, said barrier impeding impurities from diffusing from said first conductive layer through said liner,

annealing said liner and said first conductive layer in a first element ambient; and

forming a second conductive layer over said liner, wherein said barrier impedes said impurities from diffusing from said second conductive layer through said liner during said forming of said second conductive layer.

9. The process in claim 8, wherein a concentration of said material in said liner is less than an amount necessary to form a stoichiometric combination of said liner and said passivating element.

10. The process in claim 8, wherein said forming of said second conductive layer over said liner comprises a chemical vapor deposition process.

11. The process in claim 8, wherein said impurities comprise one or more of silicon impurities and fluorine impurities.

12. The process in claim 8, wherein:

said liner comprises one of tungsten, titanum, molybdenum and nickel;

said passivating agent comprises one or more of nitrogen and chlorine;

said first element comprises one or more of hydrogen, nitrogen, and ammonia; and

said second conductive layer comprises one of tungsten and copper.

13. A process of forming an integrated circuit chip comprising:

depositing a liner on a first conductive layer, a portion of said depositing being carried out in the presence of a passivating material, wherein said passivating material combines with said liner to form a barrier, said barrier impeding impurities from diffusing from said first conductive layer through said liner,

annealing said liner and said first conductive layer in a first element ambient; and

forming a second conductive layer over said liner, wherein said barrier impedes said impurities from diffusing from said second conductive layer through said liner during said forming of said second conductive layer.

14. The process in claim 13, wherein a concentration of said material in said liner is less than an amount necessary to form a stoichiometric combination of said liner and said passivating element.

15. The process in claim 13, wherein said forming of said second conductive layer over said liner comprises a chemical vapor deposition process.

16. The process in claim 13, wherein said impurities comprise one or more of silicon impurities and fluorine impurities.

17. The process in claim 13, wherein:

said liner comprises one of tungsten, titanum, molybdenum and nickel;

said passivating agent comprises one or more of nitrogen and chlorine;

said first element comprises one or more of hydrogen, nitrogen, and ammonia; and

said second conductive layer comprises one of tungsten and copper.

18. A refractory metal liner, comprising:

a barrier comprising a passivating agent, said barrier impeding a subsequent reaction of at least a top half of said refractory metal liner with an adjacent conductive layer, an amount of said passivating agent in said barrier being less than an amount necessary to form a stoichiometric combination of said refractory metal liner and said passivating agent.

19. The refractory metal liner in claim 18, wherein said barrier is positioned in a central portion of said refractory metal.

20. The refractory metal liner in claim 19, wherein said barrier impedes impurities from diffusing from said first conductive layer through said refractory metal.

21. The refractory metal liner in claim 20, wherein said impurities comprise silicon impurities.

22. The refractory metal liner in claim 19, wherein a second conductive layer is positioned over said refractory metal, said barrier impeding impurities from diffusing from said second conductive layer through said refractory metal.

23. The refractory metal liner in claim 22, wherein said impurities comprise fluorine impurities.

24. The refractory metal liner in claim 22, wherein:

said refractory metal comprises one of tungsten, titanum, molybdenum and nickel; and

said passivating agent comprises one or more of nitrogen and chlorine.

25. An electrical connection in an integrated circuit chip, said electrical connection comprising:

a first conductive layer;

a liner on said first conductive layer, said liner including a barrier, said barrier impeding impurities from diffusing from said first conductive layer through said liner; and

a second conductive layer over said liner, wherein said barrier impedes said impurities from diffusing from said second conductive layer through said liner.

26. The electrical connection in claim 25, wherein said barrier comprises a concentration of a passivating agent less than an amount necessary to form a stoichiometric combination with said liner.

27. The electrical connection in claim 26, wherein:

said refractory metal comprises one of tungsten, titanum, molybdenum and nickel;

said passivating agent comprises one or more of nitrogen and chlorine; and

said second conductive layer comprises one of tungsten and copper.

28. The electrical connection in claim 25, wherein said impurities comprise one or more of silicon impurities and fluorine impurities.

29. An integrated circuit chip comprising:

a first conductive layer;

a liner on said first conductive layer, said liner including a barrier, said barrier impeding impurities from diffusing from said first conductive layer through said liner,

a second conductive layer over said liner, wherein said barrier impedes said impurities from diffusing from said second conductive layer through said liner.

30. The integrated circuit chip in claim 29, wherein said barrier comprises a concentration of a passivating agent less than an amount necessary to form a stoichiometric combination with said liner.

31. The integrated circuit chip in claim 30, wherein:

said refractory metal comprises one of tungsten, titanum, molybdenum and nickel;

said passivating agent comprises one or more of nitrogen and chlorine; and

said second conductive layer comprises one of tungsten and copper.

32. The integrated circuit chip in claim 29, wherein said impurities comprise one or more of silicon impurities and fluorine impurities.